In the Claims:

1-36. (Cancelled)

37. A method of making an integrated circuit chip package, comprising the steps of:

a) forming a leadframe to include:

a frame;

a die pad integrally connected to the frame and defining opposed, generally planar first and second die pad surfaces, and at least one peripheral die pad side surface extending between the first and second die pad surfaces; and

a plurality of tabs integrally connected to the frame and extending toward the die pad in spaced relation thereto, each of the tabs defining opposed, generally planar first and second tab surfaces and at least one peripheral tab side surface extending between the first and second tab surfaces;

b) chemically etching the leadframe, a reentrant portion being disposed within at least portions of each of the peripheral die pad and tab side surfaces as a result of the etching of the leadframe;

c) placing an integrated circuit die upon the first die pad surface of the die pad;

d) electrically connecting the integrated circuit die to the first tab surface of each of the tabs;

e) applying an encapsulant material to the frame, the integrated circuit die, the first die pad surface of the die pad, the first tab surface of each of the tabs, and into the reentrant portions of the peripheral die pad and tab side surfaces, without covering the second surface of each of the tabs;

f) hardening the encapsulant material; and

g) singulating the encapsulated frame so that the die pad and the tabs are severed from the frame, the second surface of each of the tabs being exposed within the package.

38. The method of Claim 37 wherein step (e) comprises applying the encapsulant material such that the second die pad surface of the die pad is exposed.

39. The method of Claim 38 wherein step (f) further comprises plating the second die pad surface of the die pad and the second tab surface of each of the tabs with a metal subsequent to the hardening of the encapsulant material.

40. The method of Claim 37 wherein step (g) comprises forming orthogonal peripheral sides on the package.

41. The method of Claim 37 wherein step (g) is accomplished by a saw singulation process.

42. The method of Claim 37 wherein step (a) comprises forming the leadframe such that:

the die pad defines at least four peripheral die pad side surfaces;

each of the tabs defines at least three peripheral tab side surfaces; and

the reentrant portion is disposed within each of the at least four peripheral die pad side surfaces of the die pad and within each of the at least three peripheral tab side surfaces of each of the tabs.

43. The method of Claim 42 wherein step (a) comprises forming the reentrant portions so as to define a central peak which extends outward from each of the peripheral die pad and tab side surfaces.

44. The method of Claim 43 wherein step (a) comprises forming asperities upon the central peak extending from each of the peripheral die pad and tab side surfaces.

45. The method of Claim 42 wherein step (a) comprises forming the reentrant portions so as to define a central depression within each of the peripheral die pad and tab side surfaces.

46. The method of Claim 45 wherein step (a) comprises forming asperities within the central depression disposed in each of the peripheral die pad and tab side surfaces.

47. The method of Claim 42 wherein step (a) comprises forming the reentrant portions so as to define a rectangularly configured lip within each of the peripheral die pad and tab side surfaces.

48. A method of making an integrated circuit chip package, comprising the steps of:

a) forming a leadframe to include:

a die pad defining opposed, generally planar first and second die pad surfaces, and at least one peripheral die pad side surface extending between the first and second die pad surfaces; and

a plurality of tabs extending toward the die pad in spaced relation thereto, each of the tabs defining opposed, generally planar first and second tab surfaces and at least one peripheral tab side surface extending between the first and second tab surfaces;

b) chemically etching the leadframe, a reentrant portion being disposed within at least portions of each of the peripheral die pad and tab side surfaces as a result of the etching of the leadframe;

c) placing an integrated circuit die upon the first die pad surface of the die pad;

d) electrically connecting the integrated circuit die to the first tab surface of each of the tabs;

e) applying an encapsulant material to the integrated circuit die, the first die pad surface of the die pad, the first tab surface of each of the tabs, and into the reentrant portions of the peripheral die pad and tab side surfaces without covering the second surface of each of the tabs; and

f) hardening the encapsulant material.

49. The method of Claim 48 wherein step (e) comprises applying the encapsulant material such that the second die pad surface of the die pad is exposed.

50. The method of Claim 48 wherein step (a) comprises forming the leadframe such that:

the die pad defines at least four peripheral die pad side surfaces;

each of the tabs defines at least three peripheral tab side surfaces; and

the reentrant portion is disposed within each of the at least four peripheral die pad side surfaces of the die pad and within each of the at least three peripheral tab side surfaces of each of the tabs.

51. The method of Claim 50 wherein step (a) comprises forming the reentrant portions so as to define a central peak which extends outward from each of the peripheral die pad and tab side surfaces.

52. The method of Claim 51 wherein step (a) comprises forming asperities upon the central peak extending from each of the peripheral die pad and tab side surfaces.

53. The method of Claim 50 wherein step (a) comprises forming the reentrant portions so as to define a central depression within each of the peripheral die pad and tab side surfaces.

54. The method of Claim 53 wherein step (a) comprises forming asperities within the central depression disposed in each of the peripheral die pad and tab side surfaces.

55. The method of Claim 50 wherein step (a) comprises forming the reentrant portions so as to define a rectangularly configured lip within each of the peripheral die pad and tab side surfaces.

56. A method of making an integrated circuit chip package, comprising the steps of:

a) forming a leadframe to include:

a die pad defining opposed, generally planar first and second die pad surfaces, and at least one peripheral die pad side surface extending between the first and second die pad surfaces;

a plurality of tabs extending toward the die pad in spaced relation thereto, each of the tabs defining opposed, generally planar first and second tab surfaces and at least one peripheral tab side surface extending between the first and second tab surfaces; and

means disposed within each of the peripheral die pad and tab side surfaces for forming a mechanical interlock to a block of a hardened encapsulant material;

b) placing an integrated circuit die upon the first die pad surface of the die pad;

c) electrically connecting the integrated circuit die to the first tab surface of each of the tabs;

d) applying an encapsulant material to the integrated circuit die, the first die pad surface of the die pad, the first tab surface of each of the tabs, and into the interlock means of the peripheral die pad and tab side surfaces, without covering the second surface of each of the tabs; and

e) hardening the encapsulant material to form the block.

57. The method of Claim 56 wherein step (d) comprises applying the encapsulant material such that the second die pad surface of the die pad is exposed.

58. The method of Claim 56 wherein step (a) comprises forming the leadframe such that:

the die pad defines at least four peripheral die pad side surfaces;

each of the tabs defines at least three peripheral tab side surfaces; and

the interlock means is disposed within each of the at least four peripheral die pad side surfaces of the die pad and within each of the at least three peripheral tab side surfaces of each of the tabs.